IN THE CLAIMS

1. (Canceled)

2. (Canceled)

3. (Canceled)

4. (Canceled)

5. (Currently amended) ~~The computer system of claim 4,~~ A computer system comprising:

a system controller including a central processing unit and a memory bus controller and configured to operate in a first interface mode;

a system memory connected with the system controller through the system bus;

a NAND flash memory configured to store a system driving code, an operating system program, and user data for the computer system; and

an interface unit configured to communicate with the system controller through the system bus in the first interface mode and configured to communicate with the NAND flash memory in a second interface mode, the interface unit being synchronized with a clock signal generated in response to predetermined command information;

wherein the interface unit comprises:

a host interface unit configured to communicate with the system controller through the system bus in the first interface mode;

a register unit configured to store configuration information about the computer system, the NAND flash memory, and the command information;

a buffer unit configured to store data of the NAND flash memory;

an oscillator configured to generate the clock signal in response to the command information;

a state machine synchronized with the clock signal and configured to control an inner operation of the interface unit in response to the command information;

a NAND flash interface unit synchronized with the clock signal and configured to communicate with the NAND flash memory via the state machine in the second interface mode;

a power-up detector configured to apply a power sensing signal to the state machine when power is applied; and

an error correcting circuit synchronized with the clock signal and configured to perform an error test and correction on the data of the NAND flash memory; and

wherein the state machine comprises:

a first block configured to control operations to program the data stored in the buffer unit and predefined error correcting parity bits in the NAND flash memory;

a second block configured to control an operation to store the data read out of the NAND flash memory in the buffer unit;

a third block configured to control an operation to boot the compute system by using the system bootstrap code stored in the NAND flash memory; and

a fourth block configured to control an operation to generate the error correcting parity bits during the programming operation of the NAND flash memory and configured to control an operation to correct an error by comparing the parity bits stored in the NAND flash memory with new parity bits during the read operation of the NAND flash memory.

6. (Original) The computer system of claim 5, wherein the state machine further comprises:

a fifth block configured to control an operation to erase the data stored in the NAND flash memory; and

a sixth block configured to apply a reset command to the NAND flash memory and to a plurality of registers within the interface unit.

7. (Currently amended) The computer system of claim 1, wherein the interface unit comprises:

a first interface unit configured to communicate with the system controller through the system bus in the first interface mode;

a second interface unit synchronized with the clock signal and configured to communicate with the NAND flash memory in the second interface mode;

a storage unit configured to store information and data exchanged between the first and second interface units; and

a control unit synchronized with the clock signal and configured to control a transmission of the information and data between the first and second interface units[[.]];

wherein the control unit comprises:

a first block configured to control operations to program the data stored in the buffer unit and predefined error correcting parity bits in the NAND flash memory;

a second block configured to control an operation to store the data read out of the NAND flash memory in the buffer unit;

a third block configured to control an operation to boot the compute system by using the system bootstrap code stored in the NAND flash memory; and

a fourth block configured to control an operation to generate the error correcting parity bits during the programming operation of the NAND flash memory and configured to control an operation to correct an error by comparing the parity bits stored in the NAND flash memory with new parity bits during the read operation of the NAND flash memory.

8. (Original) The computer system of claim 7, wherein the storage unit comprises:

a register unit configured to store configuration information about the computer system, the NAND flash memory, and the command information about the NAND flash memory; and

a buffer unit configured to store data of the NAND flash memory.

9. (Original) The computer system of claim 7, wherein the interface unit further comprises a power-up detector configured to apply a power sensing signal to the state machine when power is applied.

10. (Original) The computer system of claim 9, wherein the interface unit further comprises an error correcting circuit synchronized with the clock signal and configured to perform an error test and correction on the data of the NAND flash memory.

11. (Canceled)

12. (Currently amended) The computer system of claim [[11]]7, wherein the control unit further comprises:

a fifth block configured to control an operation to erase the data stored in the NAND flash memory; and

a sixth block configured to apply a reset command to the NAND flash memory and to a plurality of registers within the interface unit.

13-18. (Cancelled)